



H55H-M5 v :A

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REVISION HISTORY:

Rev	Date	Notes
A	2009.12.01	change from H55H-M2: 1. Vcore change to PWM(4phase) + GEN 2. PWM Mos select 3. Rear IO change PS2/SPDIF location 4. LAN change to RTL8111E/8105E 5. change 1PCI/1PCIEx4 to 2*PCIEx1 6. del UP6262 use CLK GEN over voltage

IMPORTANT NOTES ABOUT THIS SCHEMATIC

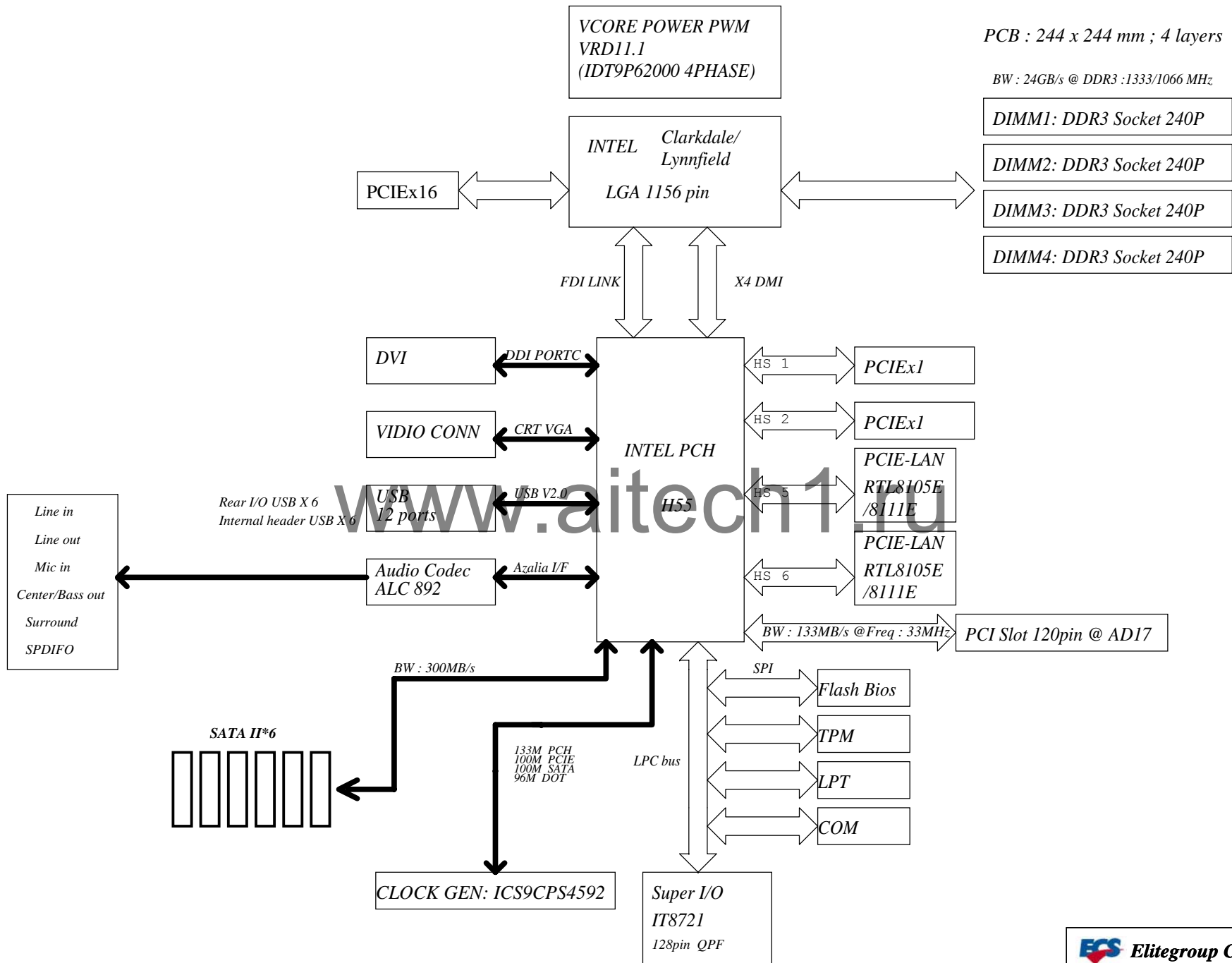
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DESIGN NOTE: Example 2) DESIGN NOTES in text for the design note to show the note inside the colored box.

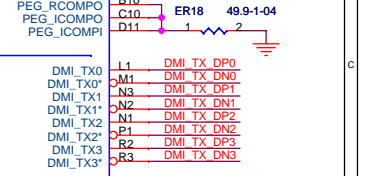
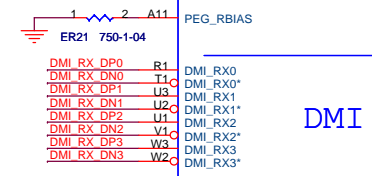
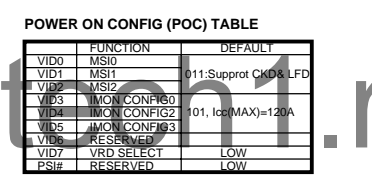
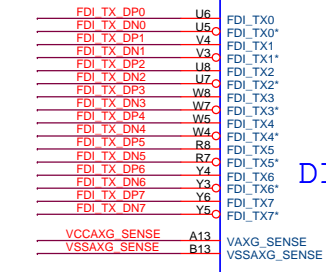
DESIGN NOTE: Example 3) DESIGN NOTES in text for the design note to show the note inside the colored box.

PCB STACK: L1:TOP
L2:VCC
L3:GND
L4:BOTTOM

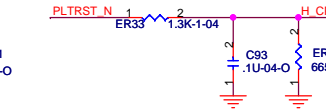
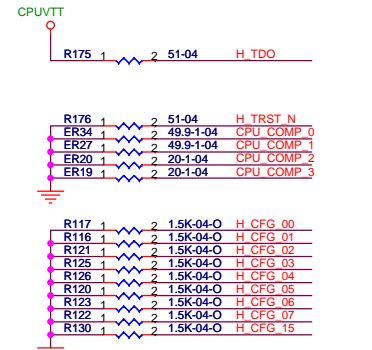
Elitegroup Computer Systems	
Title: Cover Page	
Size: Custom	Document Number: H55H-M5
Date: Thursday, December 17, 2009	Sheet: 1 of 31
Rev: A	




CPUVTT ○ — ○ CPUVTT



AK4	RSVD, A4
AK12	RSVD, A12
B3	RSVD, B3
B39	CGC, TP, NCTF
C2	RSVD, C2
D1	RSVD, D1
L12	RSVD, L12
M12	RSVD, M12
AD2	RSVD, AD2
AE2	RSVD, AE2
AH40	RSVD, AH40
AJ39	RSVD, AJ39
AK12	RSVD, AK12
AK13	RSVD, AK13
AK14	RSVD, AK14
AK15	RSVD, AK15
AK16	RSVD, AK16
AK18	RSVD, AK18
AK25	RSVD, AK25
AK26	RSVD, AK26
AK27	RSVD, AK27
AK28	RSVD, AK28
AK29	RSVD, AK29



SEL2	SEL1		PCIE CONFIG
1	1	SEL0	1 X 16
1	1	0	2 X 8

 Elitegroup Computer Systems			
Title LGA1156 CPU/GPU/PEG/DMI			
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CPUA

LGA1156

M_MAA_A0 AW18
M_MAA_A1 AY15
M_MAA_A2 AV15
M_MAA_A3 AU15
M_MAA_A4 AW14
M_MAA_A5 AY13
M_MAA_A6 AV14
M_MAA_A7 AW13
M_MAA_A8 AU14
M_MAA_A9 AW12
M_MAA_A10 AY13
M_MAA_A11 AU13
M_MAA_A12 AW11
M_MAA_A13 AU24
M_MAA_A14 AT11
M_MAA_A15 AR10

M_WE_A_N AT22
M_CAS_A_N AU22
M_RAS_A_N AT20

M_SBS_A0 AV20
M_SBS_A1 AU19
M_SBS_A2 AU12

M_SCS_A_N0 AV21
M_SCS_A_N1 AW24
M_SCS_A_N2 AU21
M_SCS_A_N3 AU23

M_SCKE_A0 AU10
M_SCKE_A1 AW10
M_SCKE_A2 AV10
M_SCKE_A3 AY10

M_ODT_A0 AV23
M_ODT_A1 AV24
M_ODT_A2 AW23
M_ODT_A3 AY24

CK_M_DDR_A_DP0 AR22
CK_M_DDR_A_DP1 AR21
CK_M_DDR_A_DP2 AP18
CK_M_DDR_A_DP3 AN18
CK_M_DDR_A_DP4 AN19
CK_M_DDR_A_DP5 AP19
CK_M_DDR_A_DP6 AN19
CK_M_DDR_A_DP7 AN19

STP18 AK22
STP19 AM22
STP11 AL23
STP9 AK23

AP10
AN10
AR11
AP11
AK9
AL9
AK11
AM11

M_DOM_A0 AJ2
M_DOM_A1 AN1
M_DOM_A2 AU1
M_DOM_A3 AN1
M_DOM_A4 AN29
M_DOM_A5 AW31
M_DOM_A6 AU36
M_DOM_A7 AT38

DRAM_RST- AV8
CPUDRV_DIMM_REFA AF3

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CPUB

LGA1156

M_MAA_B0 AU20
M_MAA_B1 AU18
M_MAA_B2 AV18
M_MAA_B3 AU17
M_MAA_B4 AU17
M_MAA_B5 AV17
M_MAA_B6 AW17
M_MAA_B7 AU16
M_MAA_B8 AT17
M_MAA_B9 AY16
M_MAA_B10 AW16
M_MAA_B11 AW16
M_MAA_B12 AW15
M_MAA_B13 AW28
M_MAA_B14 AY12
M_MAA_B15 AV11

M_WE_B_N AU26
M_CAS_B_N AW27
M_RAS_B_N AW26

M_SBS_B0 AU25
M_SBS_B1 AW25
M_SBS_B2 AV12

M_SCS_B_N0 AY27
M_SCS_B_N1 AW25
M_SCS_B_N2 AV26
M_SCS_B_N3 AV29

M_SCKE_B0 AW8
M_SCKE_B1 AY9
M_SCKE_B2 AU8
M_SCKE_B3 AV9

M_ODT_B0 AU27
M_ODT_B1 AU29
M_ODT_B2 AV27
M_ODT_B3 AU28

CK_M_DDR_B_DP0 AR17
CK_M_DDR_B_DP1 AR16
CK_M_DDR_B_DP2 AR15
CK_M_DDR_B_DP3 AR15
CK_M_DDR_B_DP4 AR15
CK_M_DDR_B_DP5 AR15
CK_M_DDR_B_DP6 AR15
CK_M_DDR_B_DP7 AR15

STP17 AM23
STP18 AM24
STP19 AL24
STP10 AK24

AR12
AT13
AN15
AP14
AM12
AN12
AP13

M_DOM_B0 AE4
M_DOM_B1 AE4
M_DOM_B2 AM7
M_DOM_B3 AT7
M_DOM_B4 AN24
M_DOM_B5 AN32
M_DOM_B6 AM33
M_DOM_B7 AK35

MCP_DDR_CMP0 AG1
MCP_DDR_CMP1 AD1
MCP_DDR_CMP2 AE1

CPUDRV_DIMM_REFB AG3

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DDR_B

SB_DQ0 AD7
SB_DQ1 AD6
SB_DQ2 AH8
SB_DQ3 AJ8
SB_DQ4 AC7
SB_DQ5 AC6
SB_DQ6 AF5
SB_DQ7 AE6
SB_DQ8 AG5
SB_DQ9 AH7
SB_DQ10 AK6
SB_DQ11 AL4
SB_DQ12 AG6
SB_DQ13 AG4
SB_DQ14 AJ7
SB_DQ15 AK7
SB_DQ16 AL6
SB_DQ17 AN5
SB_DQ18 AP6
SB_DQ19 AR5
SB_DQ20 AL5
SB_DQ21 AM5
SB_DQ22 AP5
SB_DQ23 AR5
SB_DQ24 AT6
SB_DQ25 AR7
SB_DQ26 AR9
SB_DQ27 AM8
SB_DQ28 AN8
SB_DQ29 AR6
SB_DQ30 AL8
SB_DQ31 AT9
SB_DQ32 AP23
SB_DQ33 AR25
SB_DQ34 AR26
SB_DQ35 AT23
SB_DQ36 AT22
SB_DQ37 AP25
SB_DQ38 AT26
SB_DQ39 AT32
SB_DQ40 AP31
SB_DQ41 AR33
SB_DQ42 AM32
SB_DQ43 AT31
SB_DQ44 AR31
SB_DQ45 AR34
SB_DQ46 AR33
SB_DQ47 AR35
SB_DQ48 AT36
SB_DQ49 AN33
SB_DQ50 AP36
SB_DQ51 AP34
SB_DQ52 AT35
SB_DQ53 AN34
SB_DQ54 AP37
SB_DQ55 AL35
SB_DQ56 AM35
SB_DQ57 AJ36
SB_DQ58 AJ37
SB_DQ59 AN35
SB_DQ60 AM34
SB_DQ61 AJ35
SB_DQ62 AL36
SB_DQ63

SB_WE*
SB_CAS*
SB_RAS*

SB_BS[0]
SB_BS[1]
SB_BS[2]

SB_CS[0]*
SB_CS[1]*
SB_CS[2]*
SB_CS[3]*

SB_CKE[0]
SB_CKE[1]
SB_CKE[2]
SB_CKE[3]

SB_ODT[0]
SB_ODT[1]
SB_ODT[2]
SB_ODT[3]

SB_CK[0]
SB_CK[0]*
SB_CK[1]
SB_CK[1]*
SB_CK[2]
SB_CK[2]*
SB_CK[3]
SB_CK[3]*

SB_CS[4]*
SB_CS[5]*
SB_CS[6]*
SB_CS[7]*

SB_ECC_CB[0]
SB_ECC_CB[1]
SB_ECC_CB[2]
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SB_ECC_CB[4]
SB_ECC_CB[5]
SB_ECC_CB[6]
SB_ECC_CB[7]

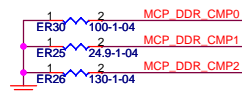
SB_DM0
SB_DM1
SB_DM2
SB_DM3
SB_DM4
SB_DM5
SB_DM6
SB_DM7

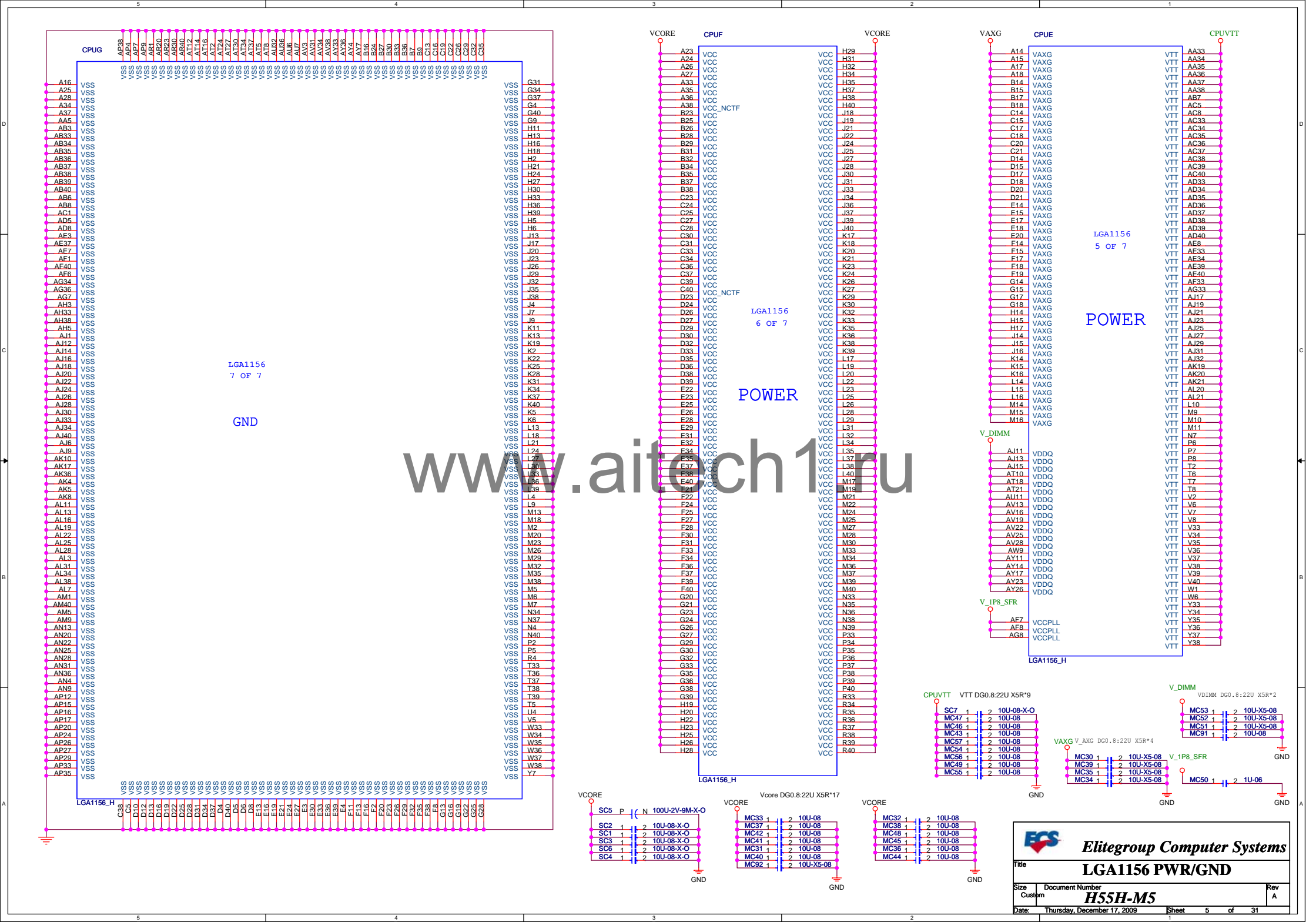
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2

SB_DM_VREFDQ

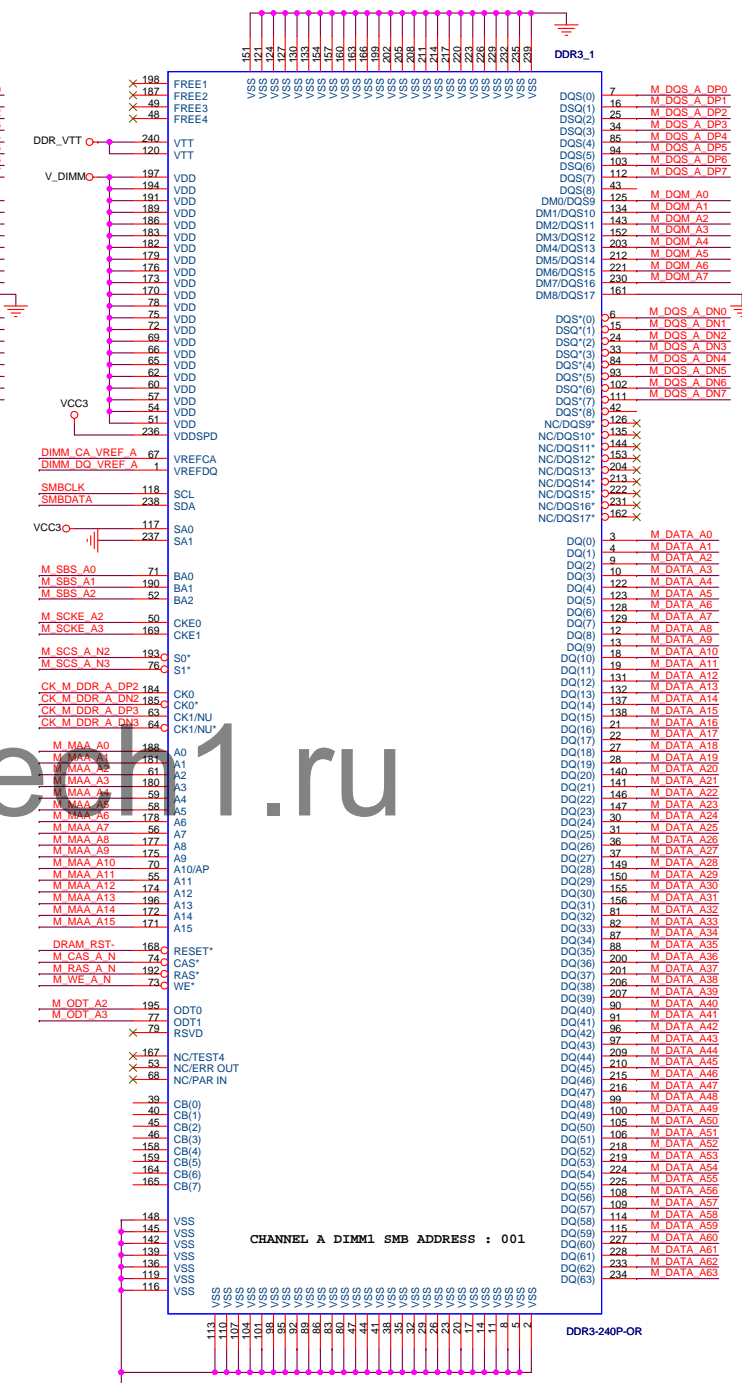
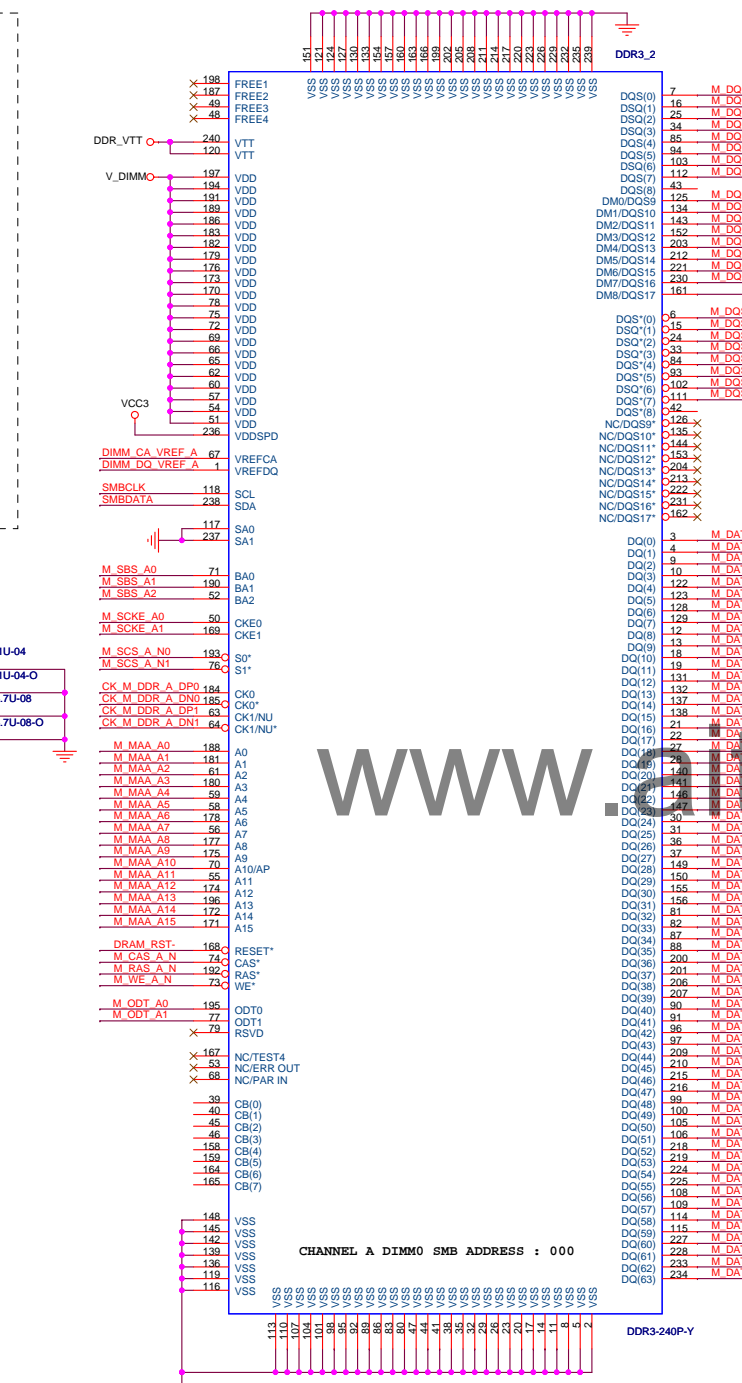
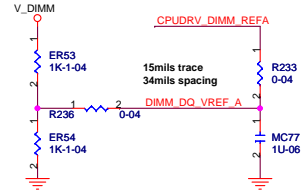
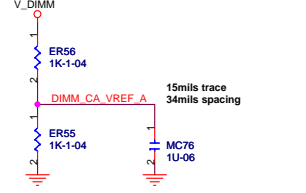
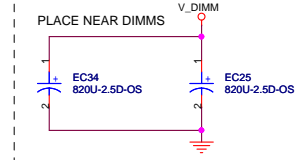
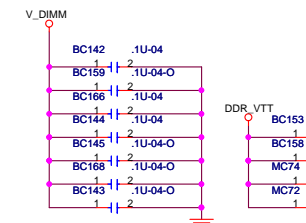
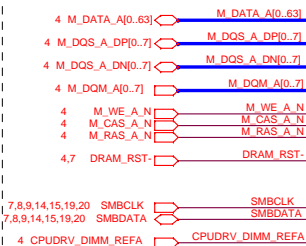
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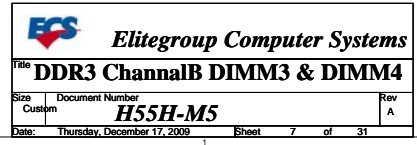


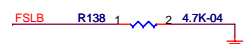
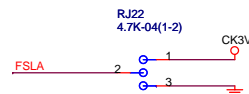
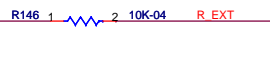
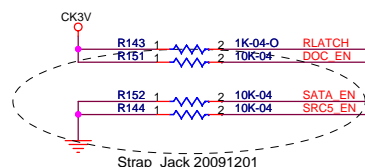
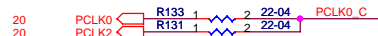
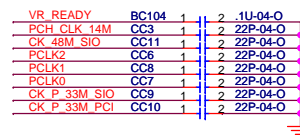
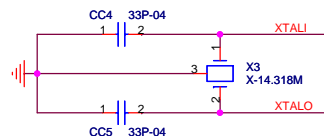
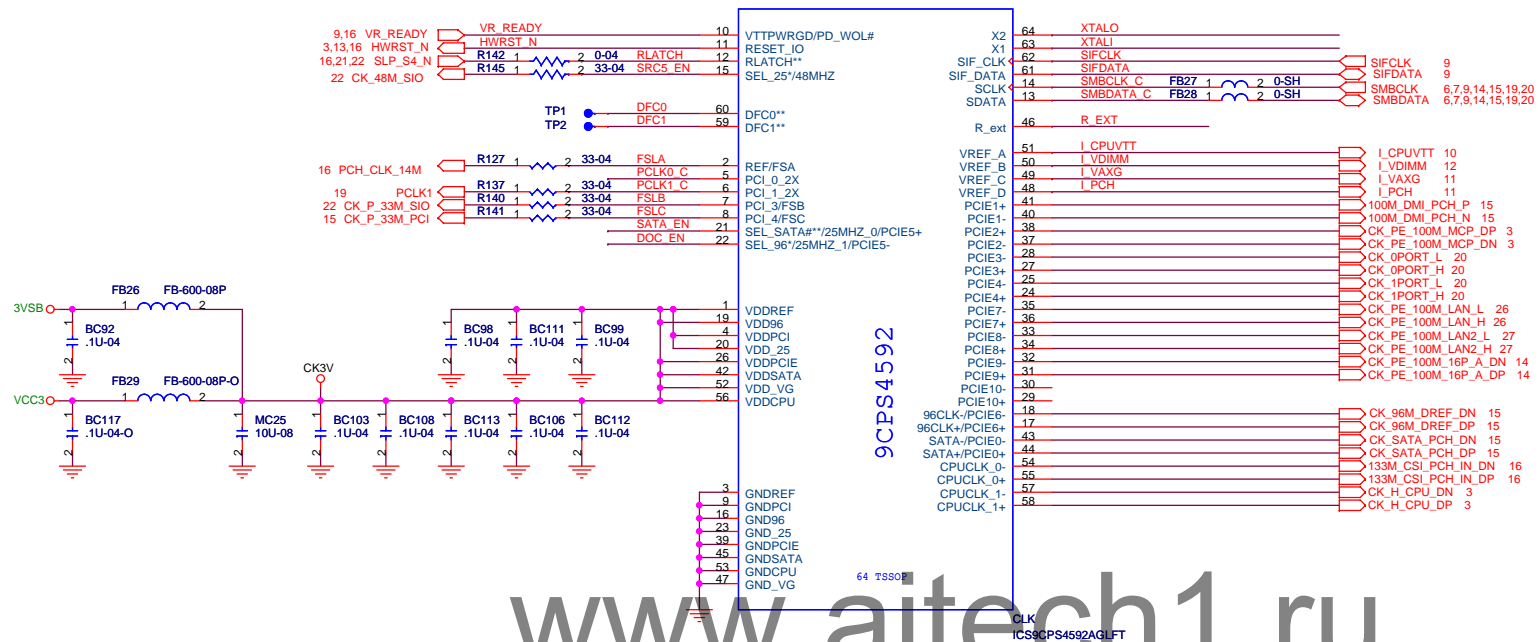


4 M_MAA_A[0..15] M_MAA_A[0..15]
 4 M_SBS_A[0..2] M_SBS_A[0..2]
 4 M_SCS_A_N[0..3] M_SCS_A_N[0..3]
 4 M_SCKE_A[0..3] M_SCKE_A[0..3]
 4 M_ODT_A[0..3] M_ODT_A[0..3]
 4 CK_M_DDR_A_DP[0..3] CK_M_DDR_A_DP[0..3]
 4 CK_M_DDR_A_DN[0..3] CK_M_DDR_A_DN[0..3]



4	M_MAA_B[0..15]		M_MAA_B[0..15]
4	M_SBS_B[0..2]		M_SBS_B[0..2]
4	M_SCs_B_N[0..3]		M_SCs_B_N[0..3]
4	M_SCKE_B[0..3]		M_SCKE_B[0..3]
4	M_ODT_B[0..3]		M_ODT_B[0..3]
4	CK_M_DDR_B_DP[0..3]		CK_M_DDR_B_DP[0..3]
4	CK_M_DDR_B_DN[0..3]		CK_M_DDR_B_DN[0..3]
4	M_DATA_B[0..63]		M_DATA_B[0..63]
4	M_DQS_B_DP[0..7]		M_DQS_B_DP[0..7]
4	M_DQS_B_DN[0..7]		M_DQS_B_DN[0..7]
4	M_DQM_B[0..7]		M_DQM_B[0..7]
4	M_WE_B_N		M_WE_B_N
4	M_CAS_B_N		M_CAS_B_N
4	M_RAS_B_N		M_RAS_B_N
4.6	DRAM_RST_		DRAM_RST_
6.8,9.14.15,19,20	SMBCLK		SMBCLK
6.8,9.14.15,19,20	SMBDATA		SMBDATA
4	CPUDRV_DIMM_REFB		CPUDRV_DIMM_REFB





FSLC,FSLB,FSLA = 001, CPU_CLK = 133MHz

FSLC (Bob2)	FSLB (Bob1)	FSLA (Bob0)	CPU MHz	PCIE MHz	SATA MHz	DOT96 MHz
0	0	1	133.33	100	100	96.00
1	0	1	100.00	100	100	96.00

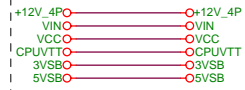
CLK GEN 阵列块 输出 Vout 为：
 当 CLK GEN 块 为 CPUVTT/Vaxg 时，

$$Vout = -Ic \cdot RFB;$$
 RFB 为：
 1. For CPUVTT, RFB = Rb = 1K;
 2. For VDMM, RFB = Rvdimm=1K
 3. For Vaxg, RFB = Rb = 1K;

PCHDMI
CPUDMI
PCIE1
PCIE2
LAN1
LAN2
PCIEX16

DOT
SATA
PCH
CPU

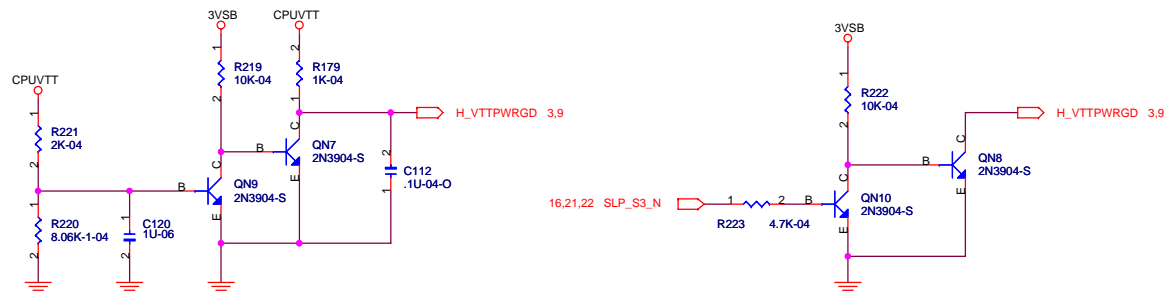
External Connection



VTT_SEL	CPUVTT
1	1.05V
0	1.10V

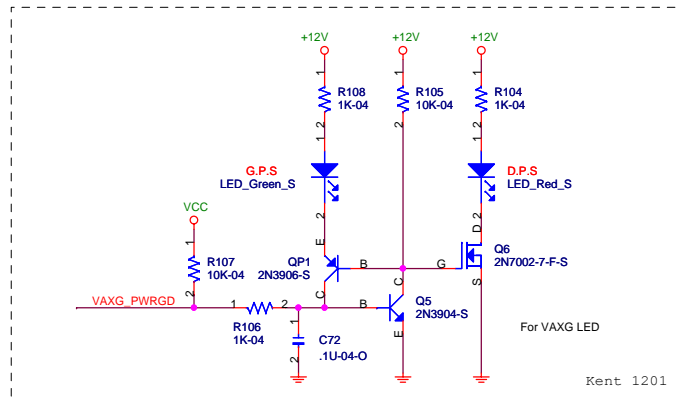
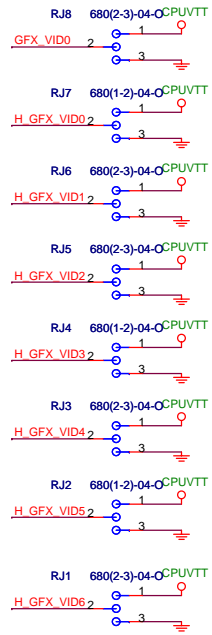
Jack 20091217

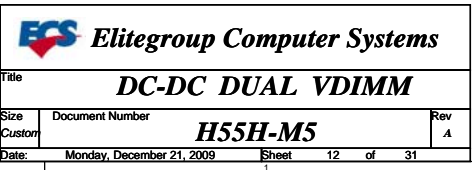
3 VTT_SEL



$I_{ocp} = - \frac{V_{ocp}}{R_{ds(on)}}$		OCP Level Selection				*
$R_{ocp} (ohm)$	open	42K	26K	10K		
$V_{ocp} (mV)$	-375	-300	-225	-150		
$I_{ocp} (A)$	125	100	75	50		

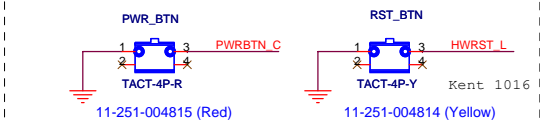
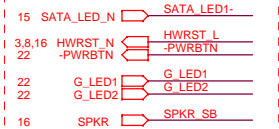
$R_{ds(on)} = 3m\ Ohm$



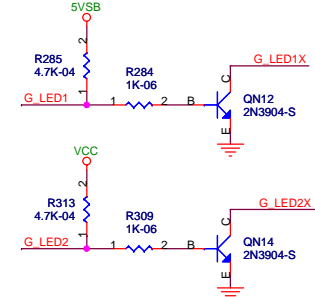
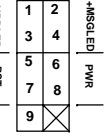


FRONT PANEL

External Connection

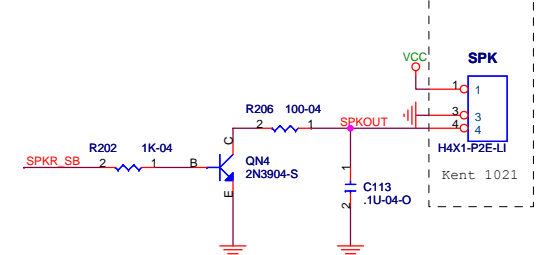


F. PANEL



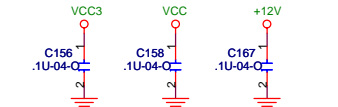
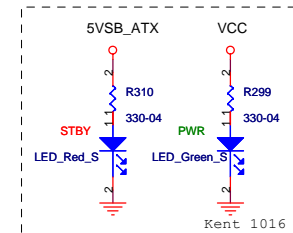
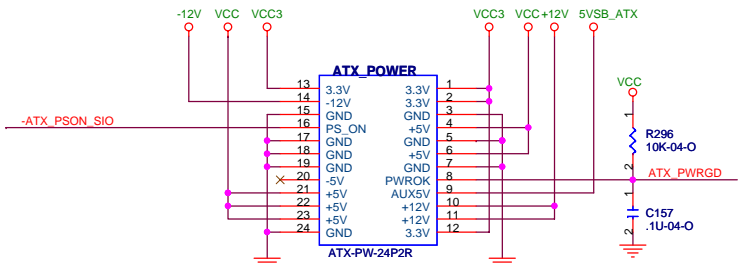
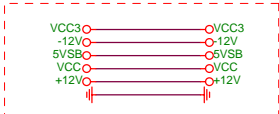
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF

B: Blinking



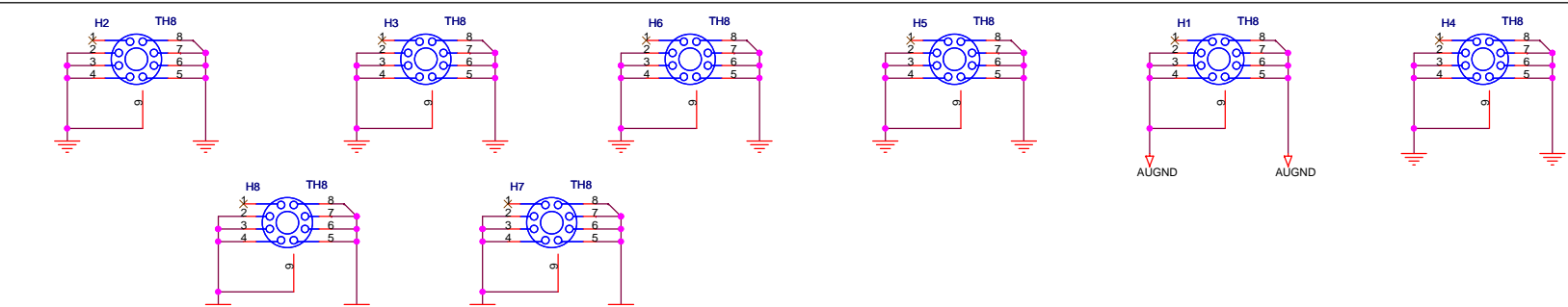
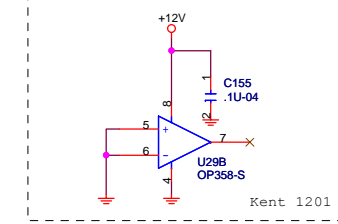
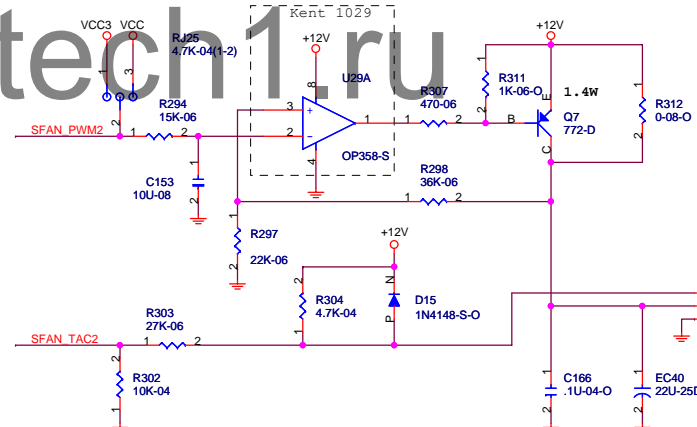
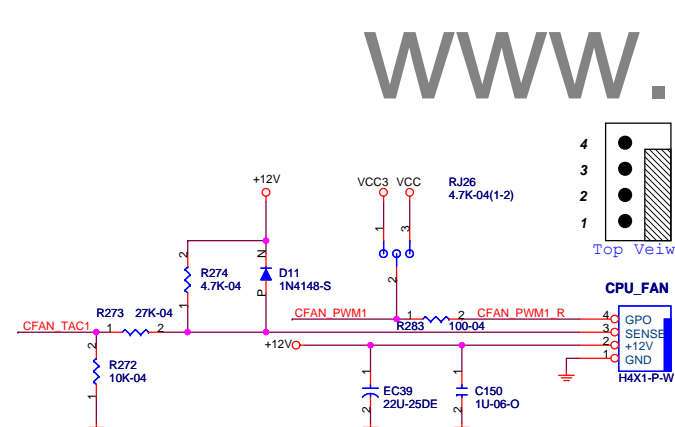
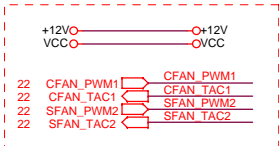
POWER CONNECTOR

External Connection



FAN

External Connection



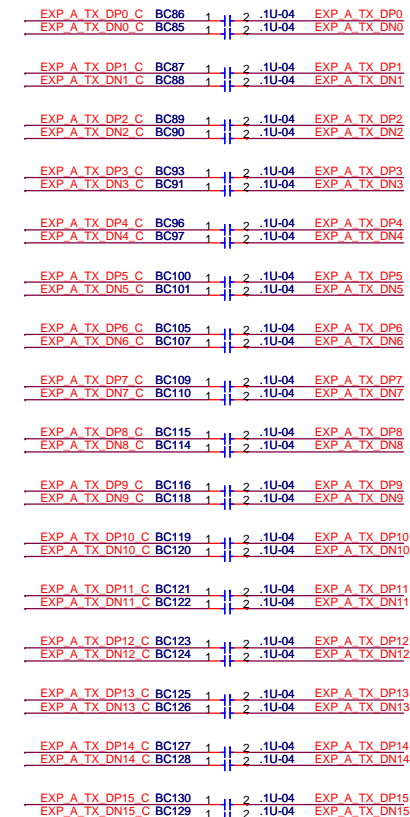
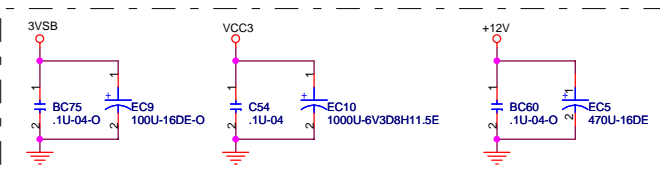
3VSB VCC3 +12V 3VSB

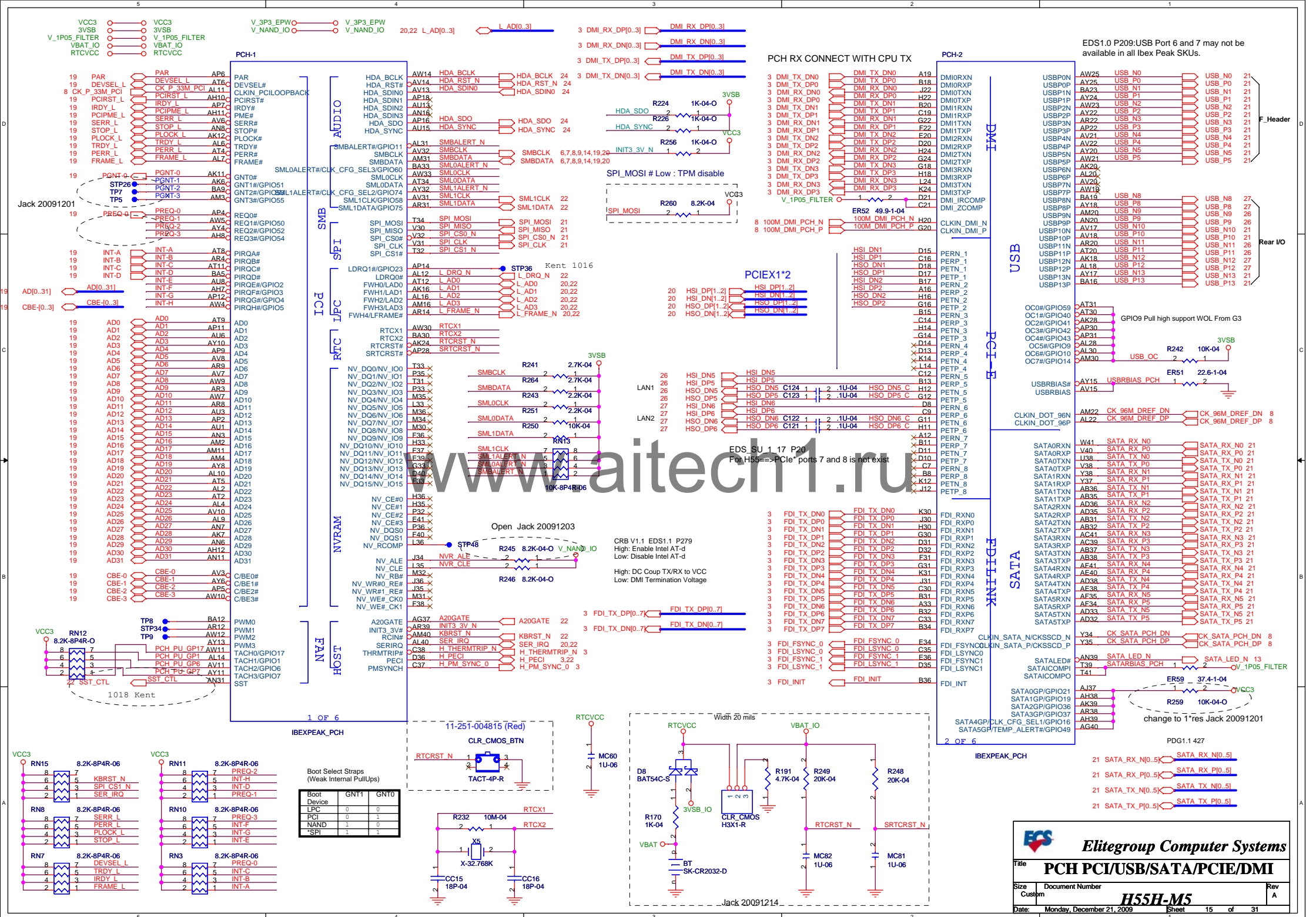
EXP_A_RX_DP[0..15] EXP_A_RX_DN[0..15] EXP_A_TX_DP[0..15] EXP_A_TX_DN[0..15]

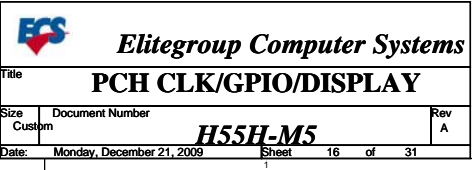
CK_PE_100M_16P_A_DN CK_PE_100M_16P_A_DP SMBCLK SMBDATA

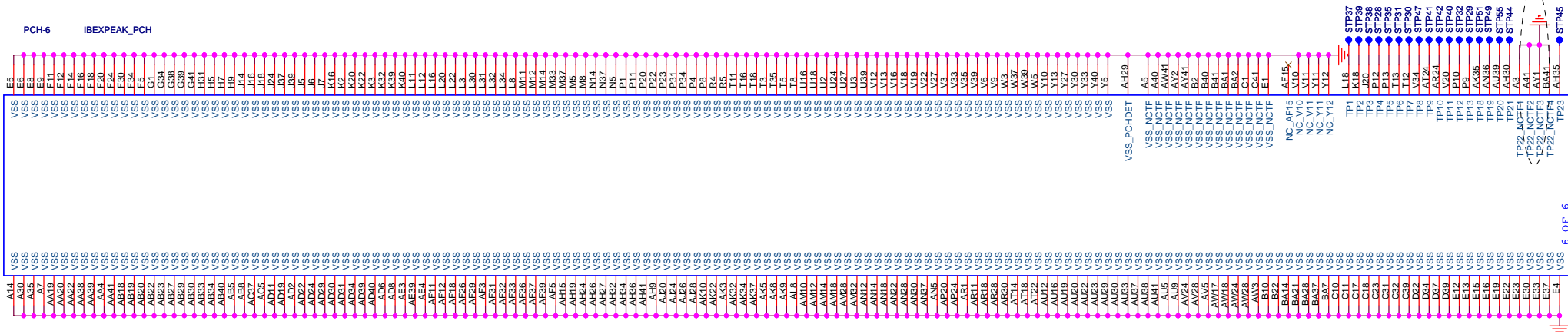
67,8,9,15,19,20 67,8,9,15,19,20 20,22 16,20,26,27

-PCI_RSTY -PCI_RSTY PCIE_WAKE_L PCIE_WAKE_L

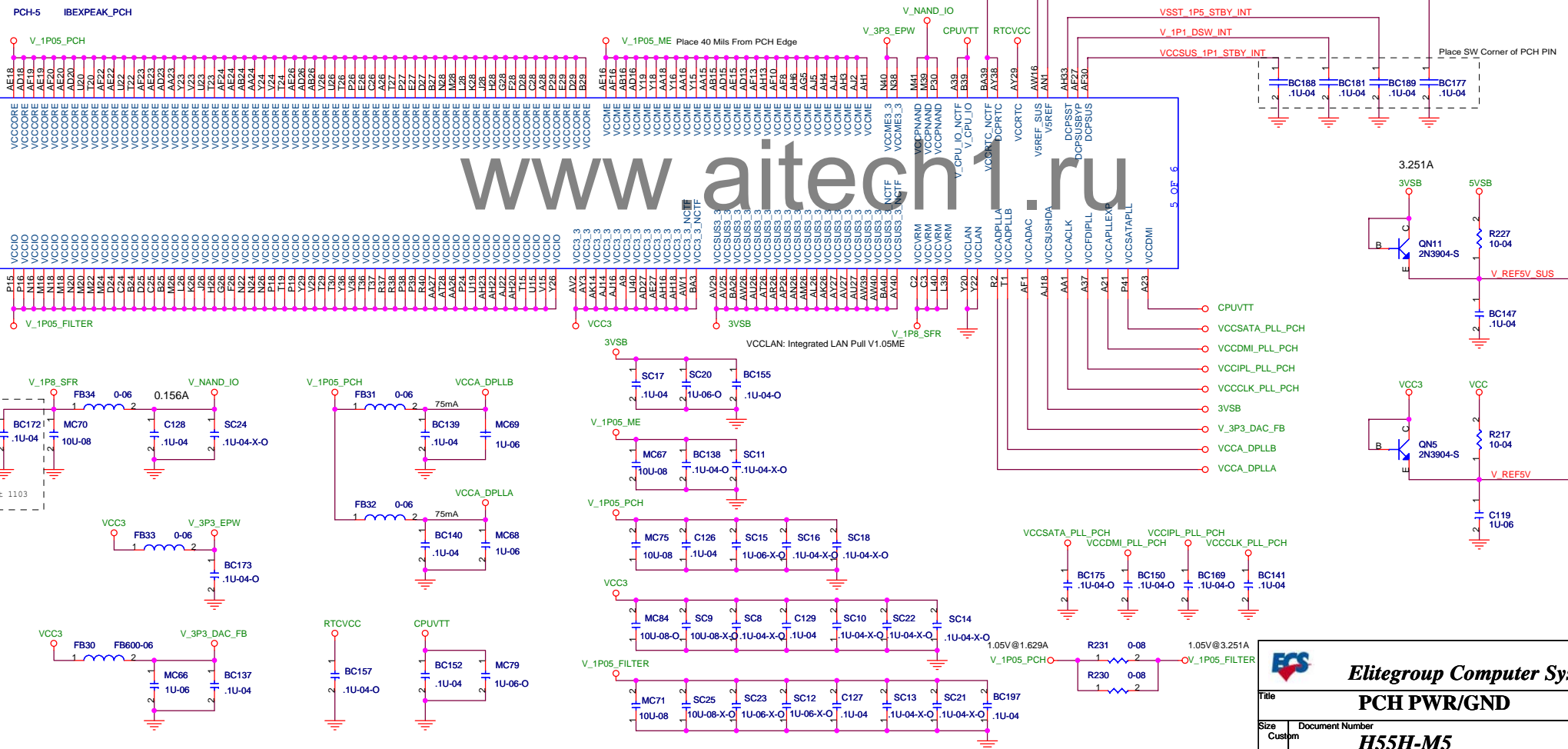






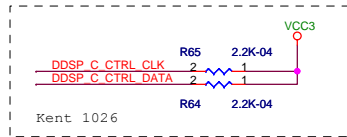


PCH-5 IBEXPEAK PCH

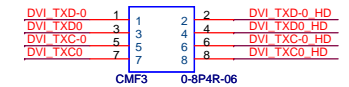


Pin connections for the DVI connector:

- Pin 16: DDSP_C_TX_DP[0..3] (Blue)
- Pin 15: DDSP_C_TX_DN[0..3] (Blue)
- Pin 14: DDSP_C_CTRL_CLK (Blue)
- Pin 13: DDSP_C_CTRL_DATA (Blue)
- Pin 12: DVI_DET (Blue)
- Pin 11: VCC3 (Green)
- Pin 10: VCC (Red)
- Pin 9: VCC (Red)
- Pin 8: VCC (Red)
- Pin 7: VCC (Red)
- Pin 6: VCC (Red)
- Pin 5: VCC (Red)
- Pin 4: VCC (Red)
- Pin 3: VCC (Red)
- Pin 2: VCC (Red)
- Pin 1: VCC (Red)



The schematic diagram illustrates the connection of the DDSP C module to the ASM1442 module. The top section shows the pin header for the DDSP C module, with signals for TX (C34 to C42), CTRL (CLK, DATA, DET), and control signals (OE#, DDC_EN, OC_3, OC_0, OC_1, OC_2, EQ_0, EQ_1, Thermal_Pad). The right side shows the connection to the ASM1442 module, including VCC3V, GND, and various control signals (DVI_TXD-2, DVI_TXD-1, DVI_TXD-0, DVI_TXC-0, DVI_TXC-1, DVI_TXC-2, DDCCLK, DDCDATA, HPLV_DVI). The bottom section shows the connection to the VCC3V and GND pins of the ASM1442 module, including a fuse F1 and a diode D1.



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16 VGA_RED ROUT

15 VGA_GREEN GOUT

14 VGA_BLUE BOUT

13

12

11

10 HSYNC

9 VSYNC

8

7

6

5

4

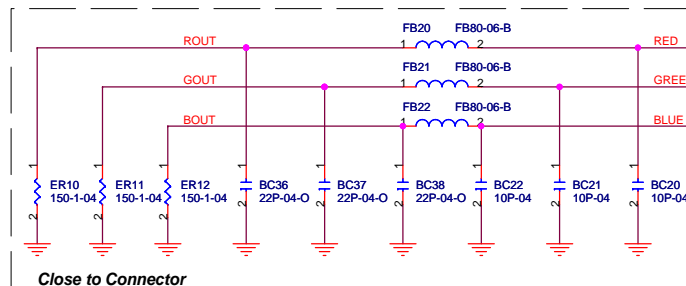
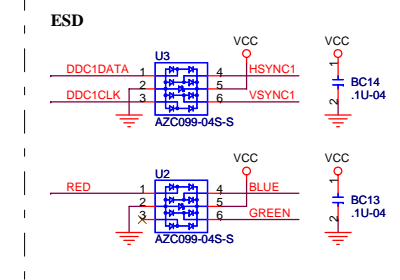
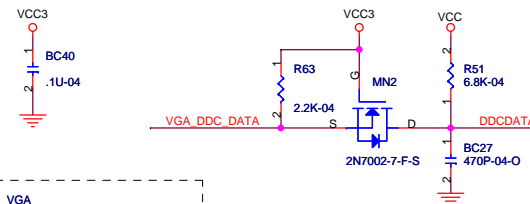
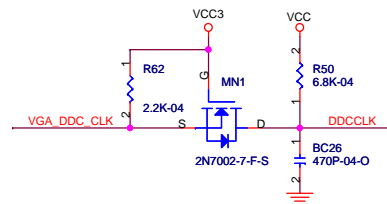
3

2

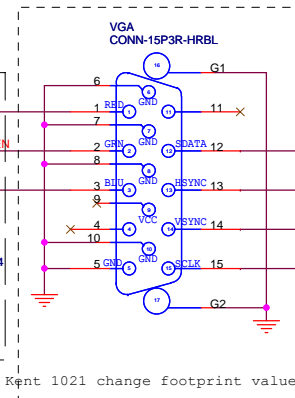
1

16 VGA_DDC_DATA VGA DDC DATA

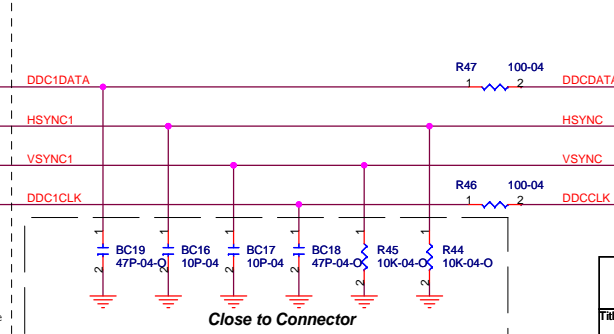
15 VGA_DDC_CLK VGA DDC CLK



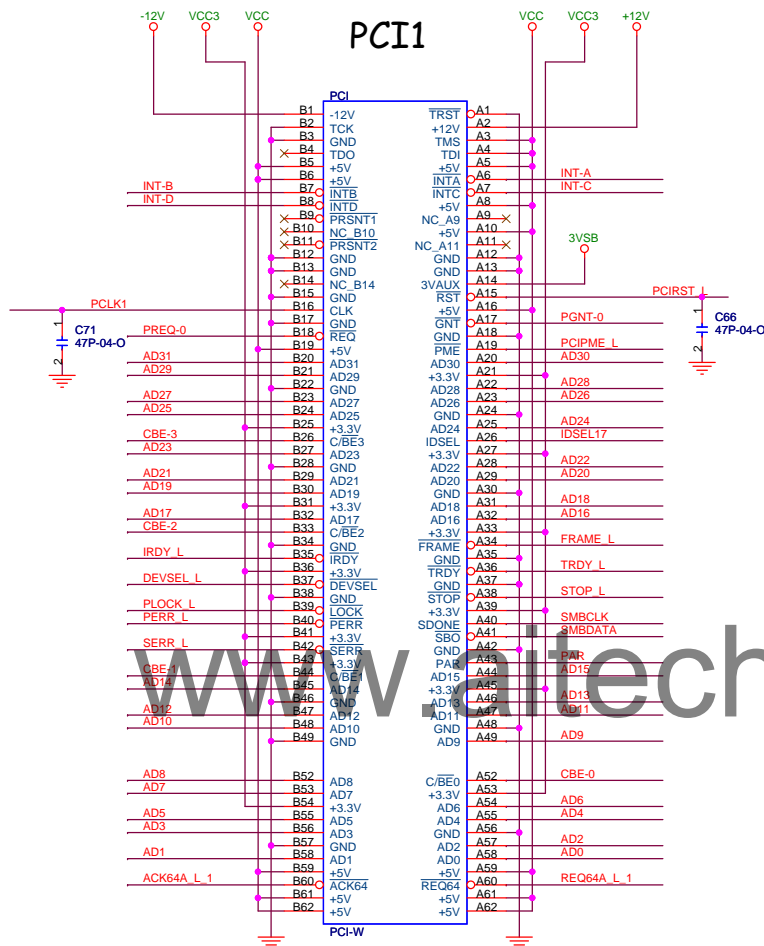
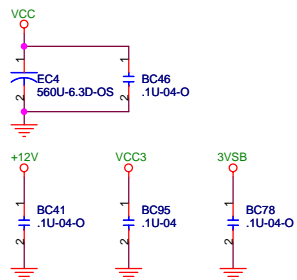
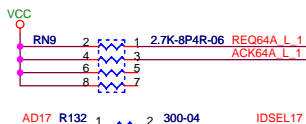
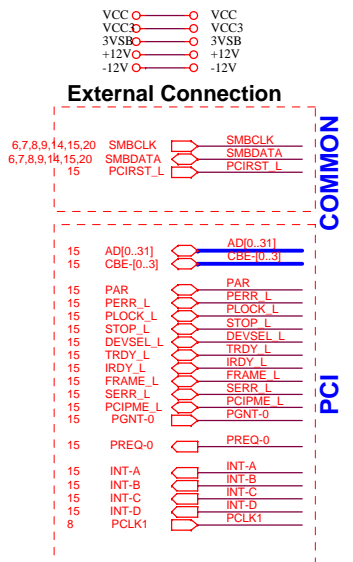
Close to Connector



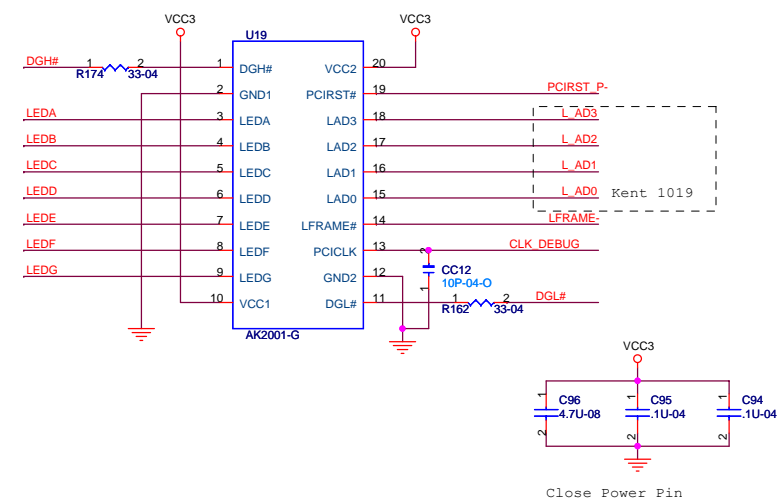
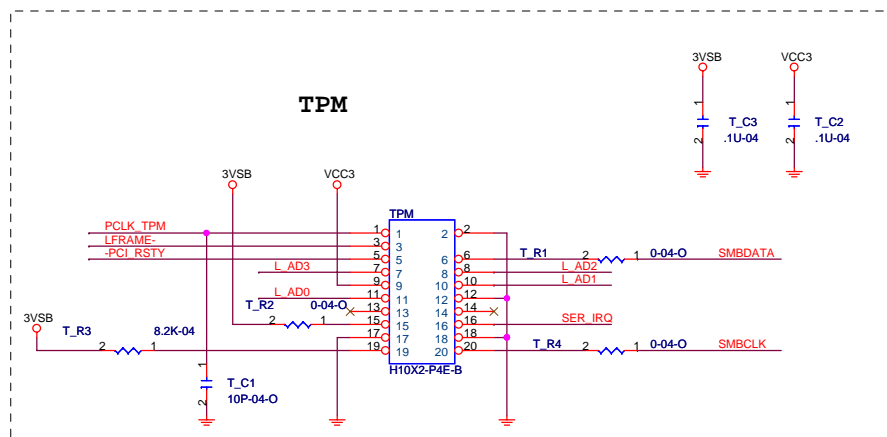
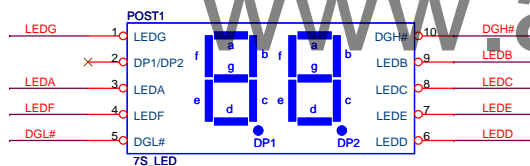
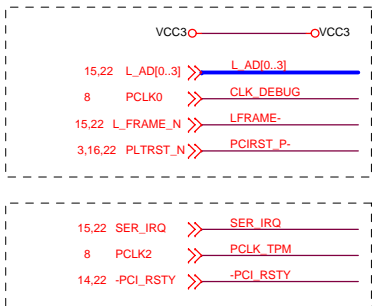
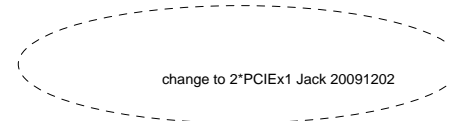
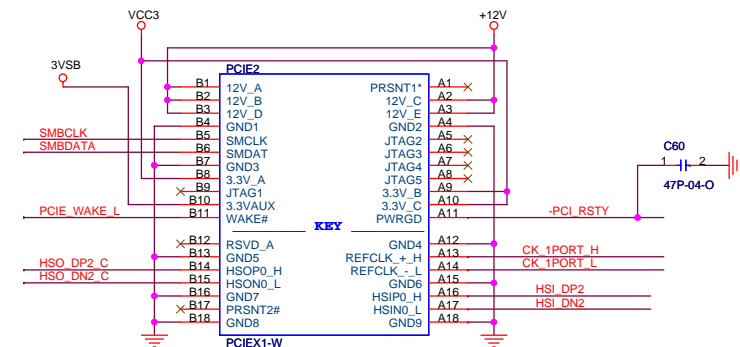
Kent 1021 change footprint value



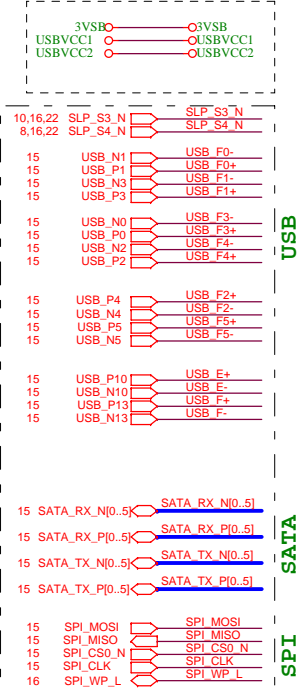
Close to Connector



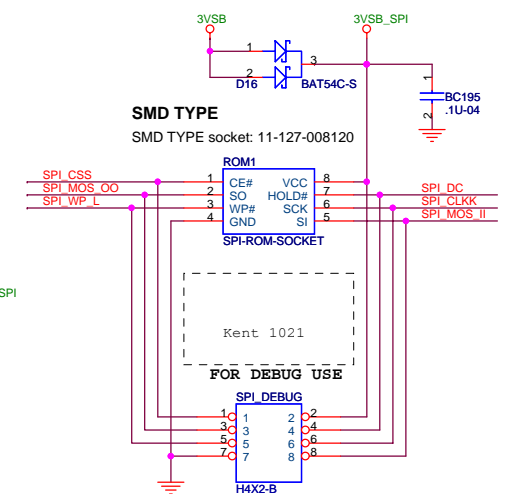
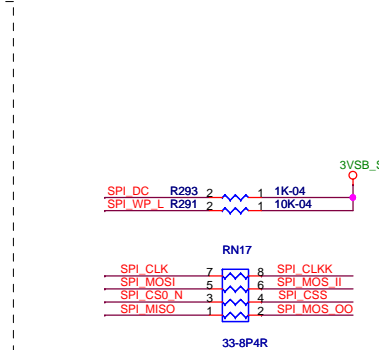
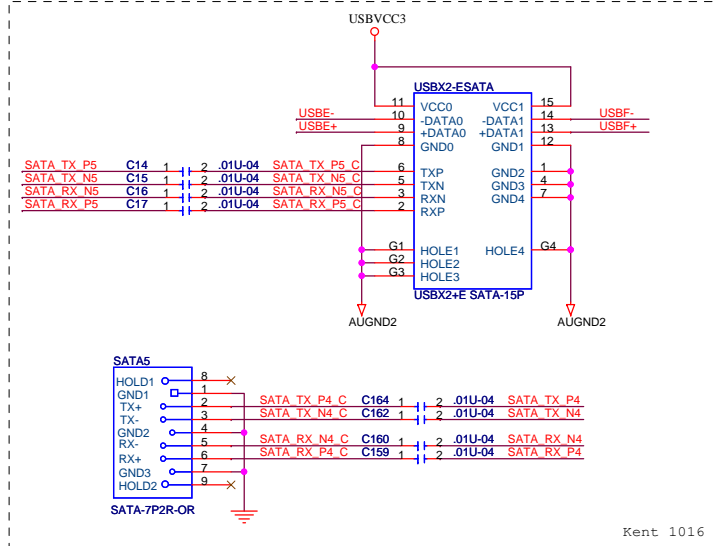
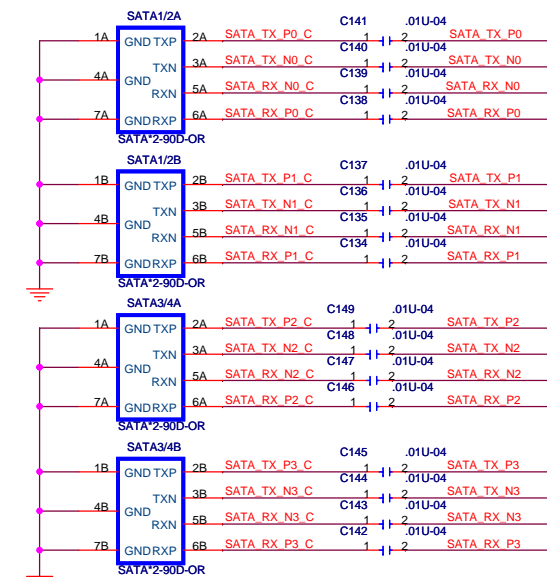
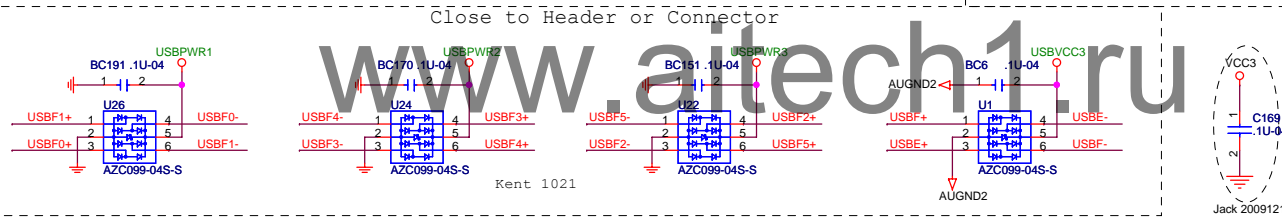
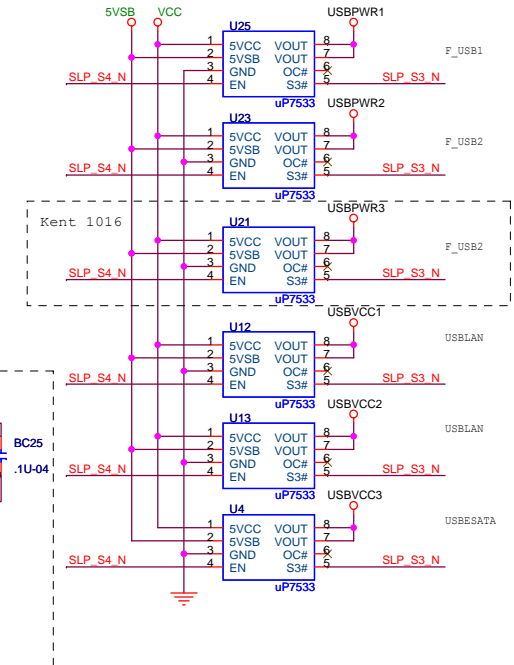
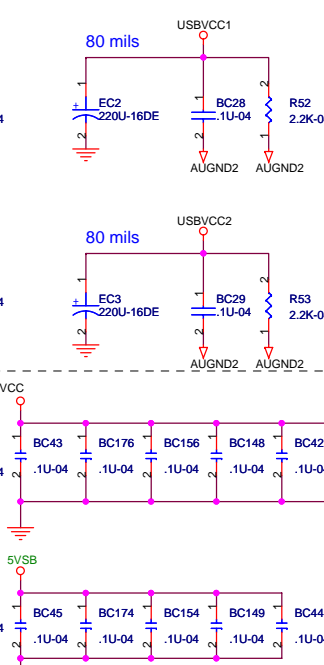
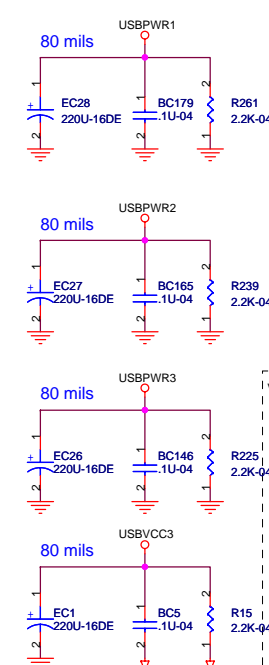
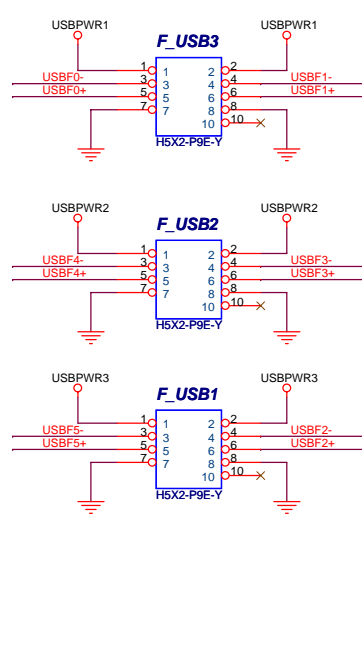
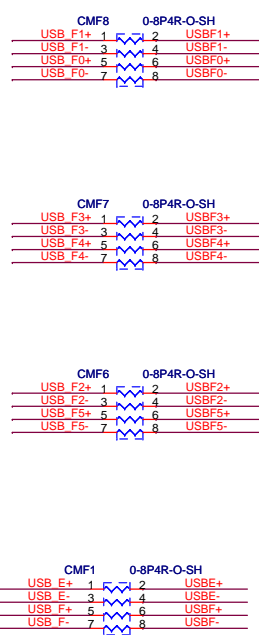
15	HSI_DP[1..2]		HSI_DP[1..2]
15	HSI_DN[1..2]		HSI_DN[1..2]
15	HSO_DP[1..2]		HSO_DP[1..2]
15	HSO_DN[1..2]		HSO_DN[1..2]
14,22	-PCI_RSTY		-PCI_RSTY
14,16,26,27	PCIE_WAKE_L		PCIE_WAKE_L
6,7,8,9,14,15,19	SMBCLK		SMBCLK
6,7,8,9,14,15,19	SMBDATA		SMBDATA
8	CK_1PORT_H		CK_1PORT_H
8	CK_1PORT_L		CK_1PORT_L
8	CK_0PORT_H		CK_0PORT_H
8	CK_0PORT_L		CK_0PORT_L



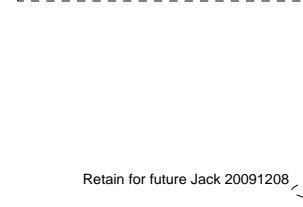
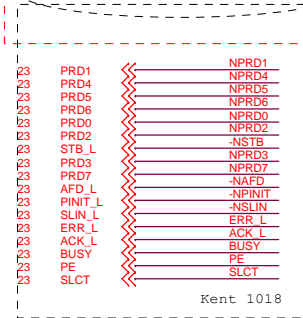
External Connection



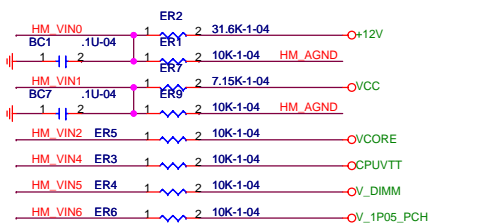
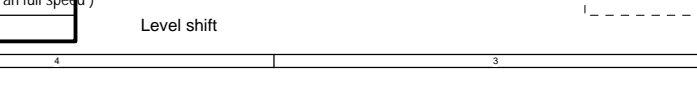
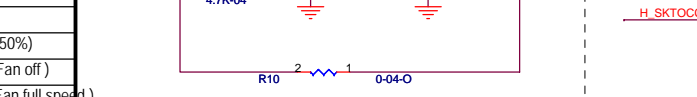
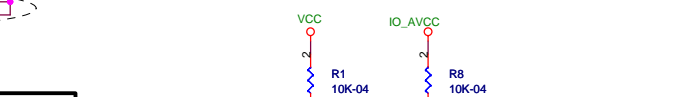
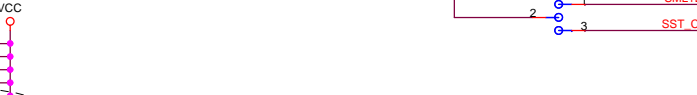
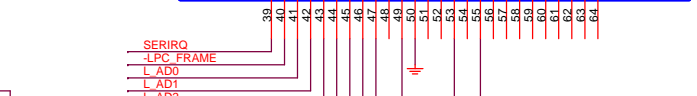
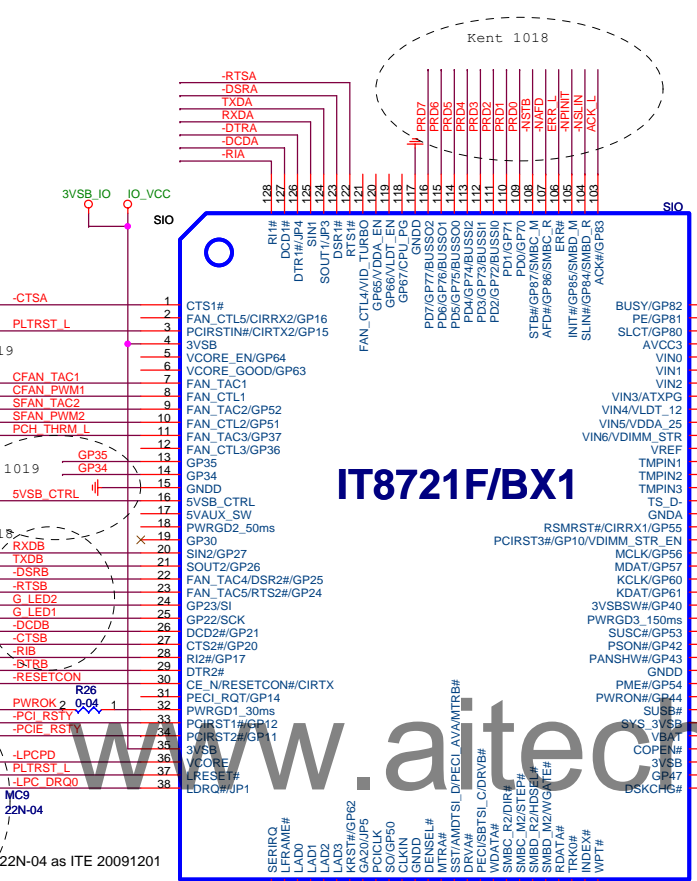
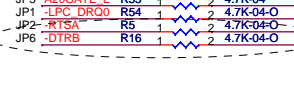
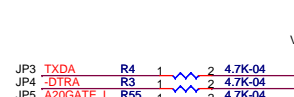
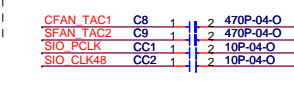
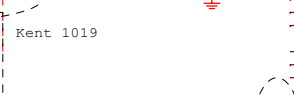
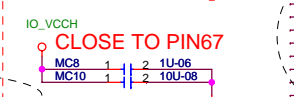
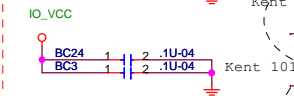
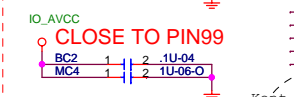
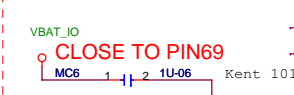
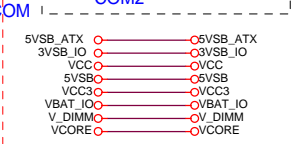
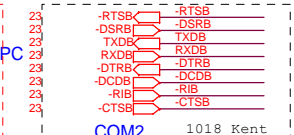
FRONT_SIDE



16	LPCPME_L	LPCPME_L
15	L_DRQ_N	-LPC_DRQ0
15,20	L_FRAME_N	-LPC_FRAME
15,20	L_AD[0:3]	-L_AD[0:3]
23	-RTSA	-RTSA
23	-DSRA	-DSRA
23	TXDA	TXDA
23	RXDA	RXDA
23	-DTRA	-DTRA
23	-DCDA	-DCDA
23	-RIA	-RIA
23	-CTSA	-CTSA
16	RSMRST_N	RSMRST_N
16	-PWRBTN	-PWRBTN
16	PWRBTN_N	-PWRON
10,16,21	SLP_S3_N	-SLP3
8,16,21	SLP_S4_N	-SLP4_L
13	-ATX_PSON_SIO	-ATX_PSON_SIO
13	ATX_PWRGD	ATX_PWRGD
16	PWROK	PWROK
16	PLTRST_L	PLTRST_L
3,16,20	PLTRST_N	-PCI_RSTY
14,20	-PCI_RSTY	-PCI_RSTY
26,27	-PCIE_RSTY	-SST_CTL
15	SST_CTL	-KB_RST
15	KBRST_N	A20GATE_L
15	A20GATE	SERIRQ
15,20	SER_IRQ	-3VSB5W
12	-3VSB5W	PEQ
3,15	H_PECI	CFAN_TAC1
13	CFAN_TAC1	CFAN_PWM1
13	CFAN_PWM1	CFAN_TAC2
13	SFAN_TAC2	SFAN_PWM2
13	SFAN_PWM2	G_LED1
23	G_LED1	G_LED2
23	G_LED2	KCLK
23	KCLK	KDATA
23	KDATA	MCLK
23	MCLK	MDATA
23	MDATA	SIO_PCLK
8	CK_P_33M_SIO	SIO_CLK48
8	CK_48M_SIO	
3	H_SKTOCCN	H_SKTOCCN
15	SML_CLK	SMCLK
15	SML_IDATA	SMLIDATA
16	THERMAL_ALERT	PCH_THRM_L



	Symbol	value	Description
JP3 Pin 124	Flashseg1_EN	*1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 126	K8PWR_EN	*1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	*11	The default value of EC Index 15h/16h/17h is 7Fh (50%)
		10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 40h



* HM_VIN2 for VCORE * HM_VIN5 for V_DIMM
* HM_VIN4 for CPU_VTT * HM_VIN6 for V_1P05_PCH

BIOS SELECTION HI: LO:

VCC3

RJ28 4.7K-04(2-3)

GP35 1 2 3

3

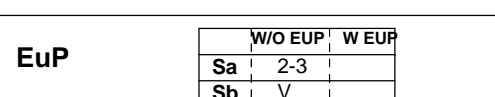
BIOS SELECTION HI: LO:

VCC3

RJ29 4.7K-04(2-3)

GP34 1 2 3

3

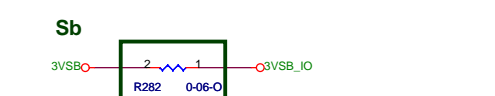


	W/O EUP	W EUP
Sa	2-3	
Sb	V	
Sc	X	
Sd	X	

page 12

Sa	2 3	
Sb	V	
Sc	X	
Sd	X	

page 12



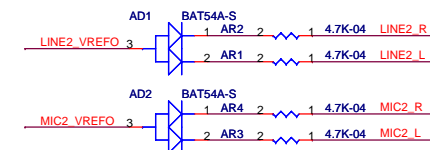
The diagram illustrates the pin connections for the AC97 Header Judgement GPI to the South Bridge. It shows a series of pins on the left and their corresponding connections on the right. The connections are as follows:

- 5VSB is connected to 5VSB.
- VCC is connected to VCC.
- +12V is connected to +12V.
- VCC3 is connected to VCC3.
- 15 HDA_RST_N is connected to AZ_RST-.
- 15 HDA_BCLK is connected to AZ_BIT_CLK.
- 15 HDA_SYNC is connected to AZ_SYNC.
- 15 HDA_SDINO is connected to AZ_SDAIN.
- 15 HDA_SDO is connected to AZ_SDOOUT.
- AGND is connected to AUGND.
- 16,25 FRONT_AUD_DET is connected to FRONT_AUD_DET.

For AC97 Header Judgement
GPI to South Bridge

Kent 1019

CODEC



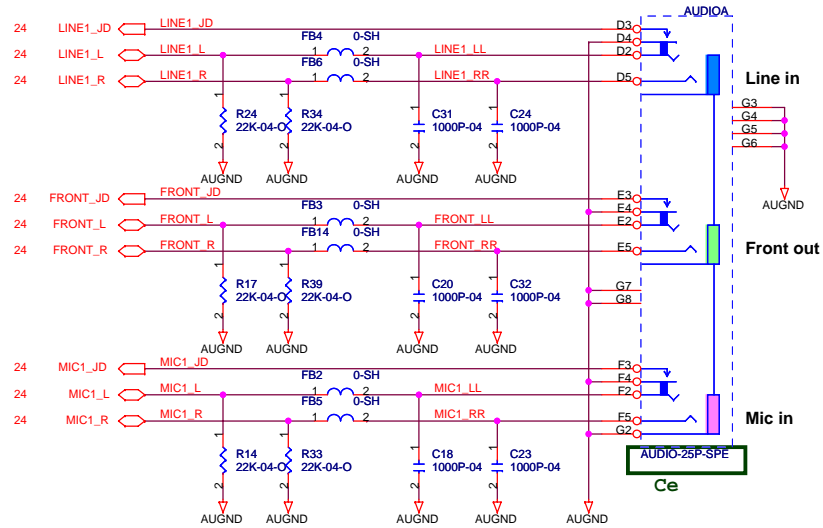
The diagram shows two network connections, NetA and NetB, to a central block labeled "Place near codec".

NetA: This network has four input lines (AER5, AER7, AER6, AER8) and four output lines (FRONT_JD, LINE1_JD, MIC1_JD, SURR_JD). Each line is labeled with a value of 25. The input lines are connected to the "Place near codec" block with the following values: AER5 (5.1K-1-04), AER7 (10K-1-04), AER6 (20K-1-04), and AER8 (39.2K-1-04). The output lines are connected to the "Place near codec" block with the following values: FRONT_JD (10K-1-04), LINE1_JD (10K-1-04), MIC1_JD (10K-1-04), and SURR_JD (10K-1-04).

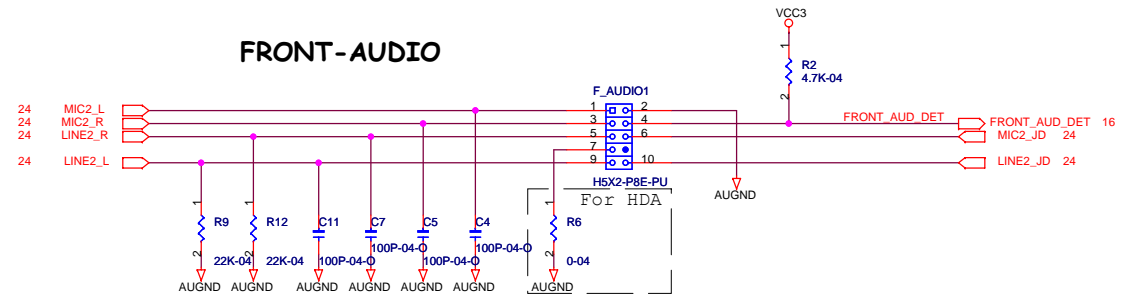
NetB: This network has four input lines (AER1, AER3, AER4) and four output lines (CEN_JD, MIC2_JD, LINE2_JD). Each line is labeled with a value of 25. The input lines are connected to the "Place near codec" block with the following values: AER1 (10K-1-04), AER3 (20K-1-04), and AER4 (39.2K-1-04). The output lines are connected to the "Place near codec" block with the following values: CEN_JD (10K-1-04), MIC2_JD (10K-1-04), and LINE2_JD (10K-1-04).

For HDA

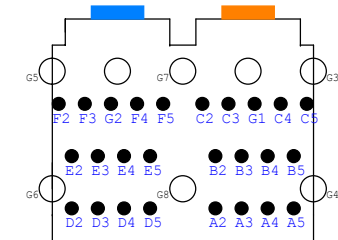
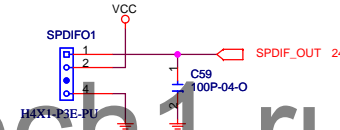
REAR-AUDIO



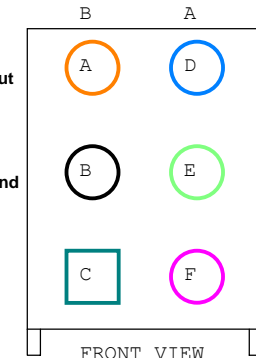
FRONT-AUDIO



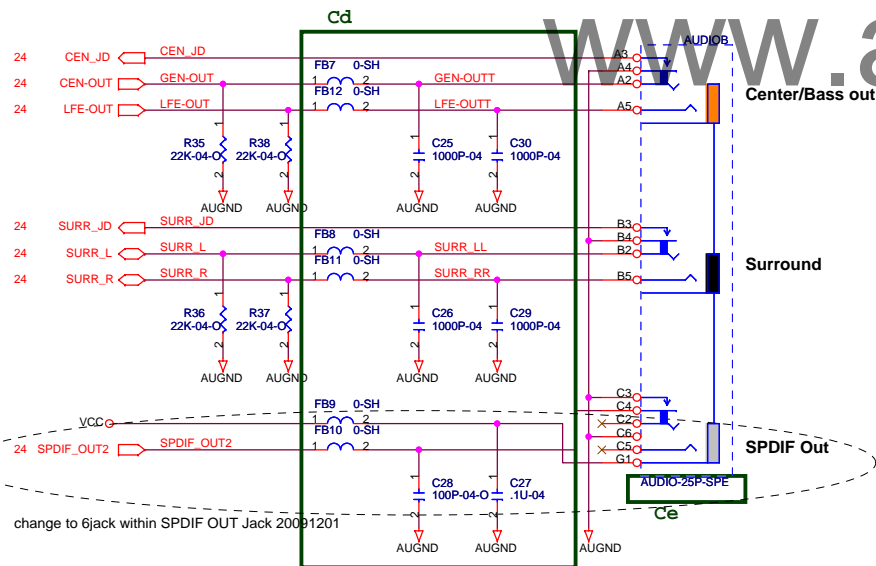
SPDIF-OUT



TOP VIEW

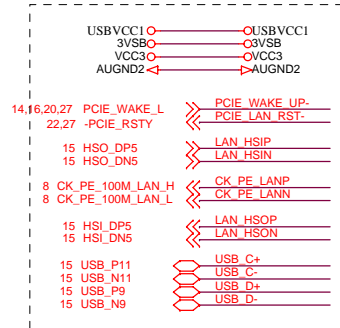


FRONT VIEW



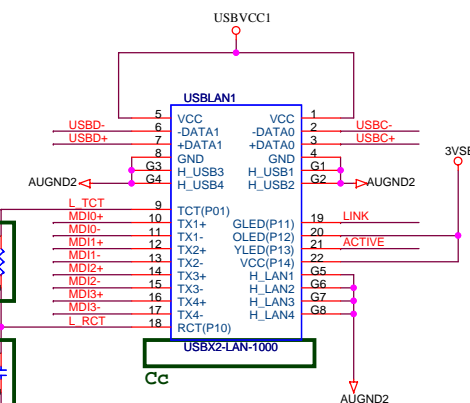
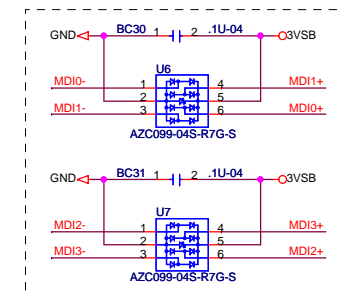
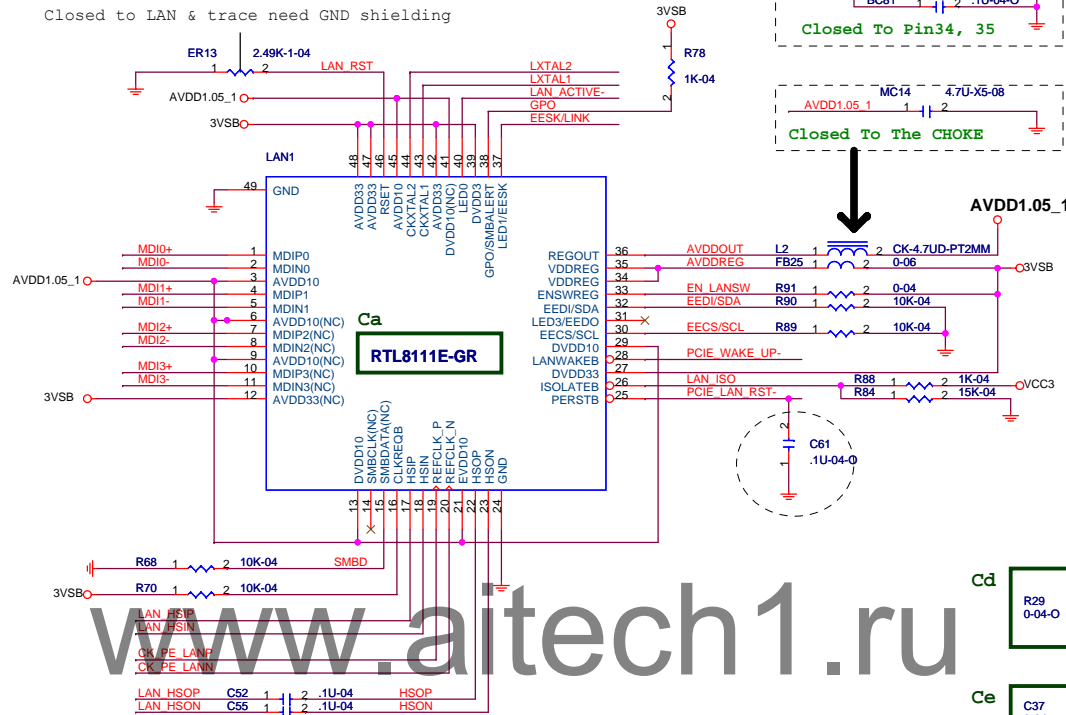
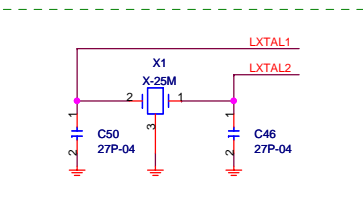
change to 6jack within SPDIF OUT Jack 20091201

External Connection



最も重要:

LAN_HSOP/N叫锁 SB PCIE RX狼
LAN_HSIP/N叫锁 SB PCIE TX狼
LAN_HSIP/N SB PCIE Tx狼璜瘳累AC coupling cap

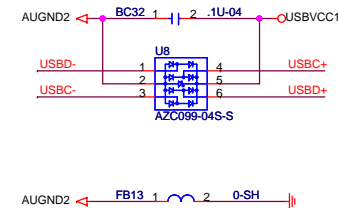
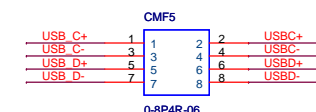
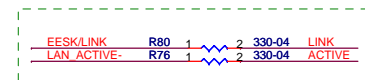
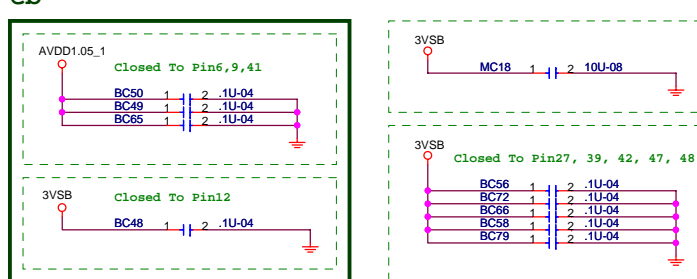


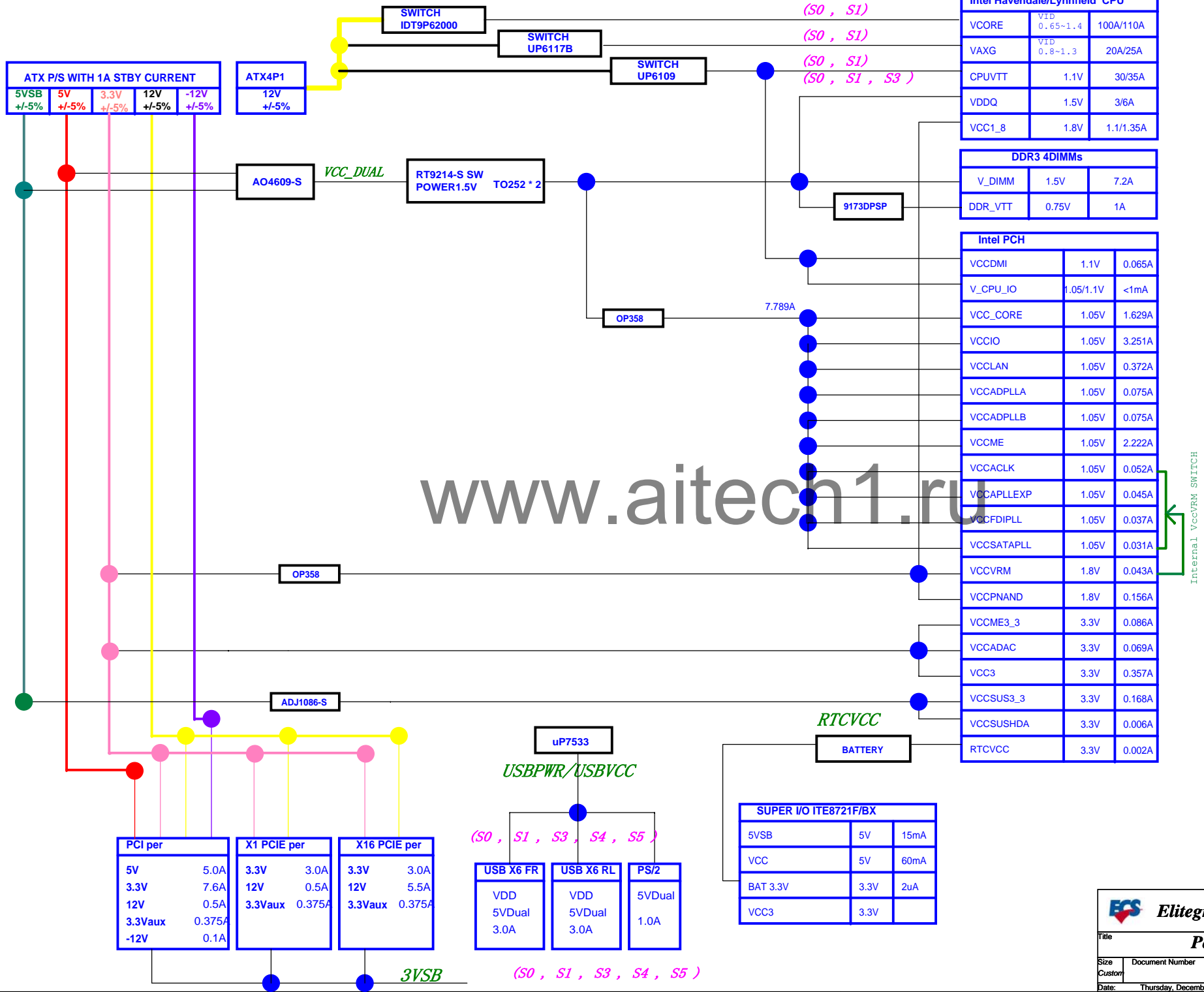
Link: Green on
Active: Yellow blinking

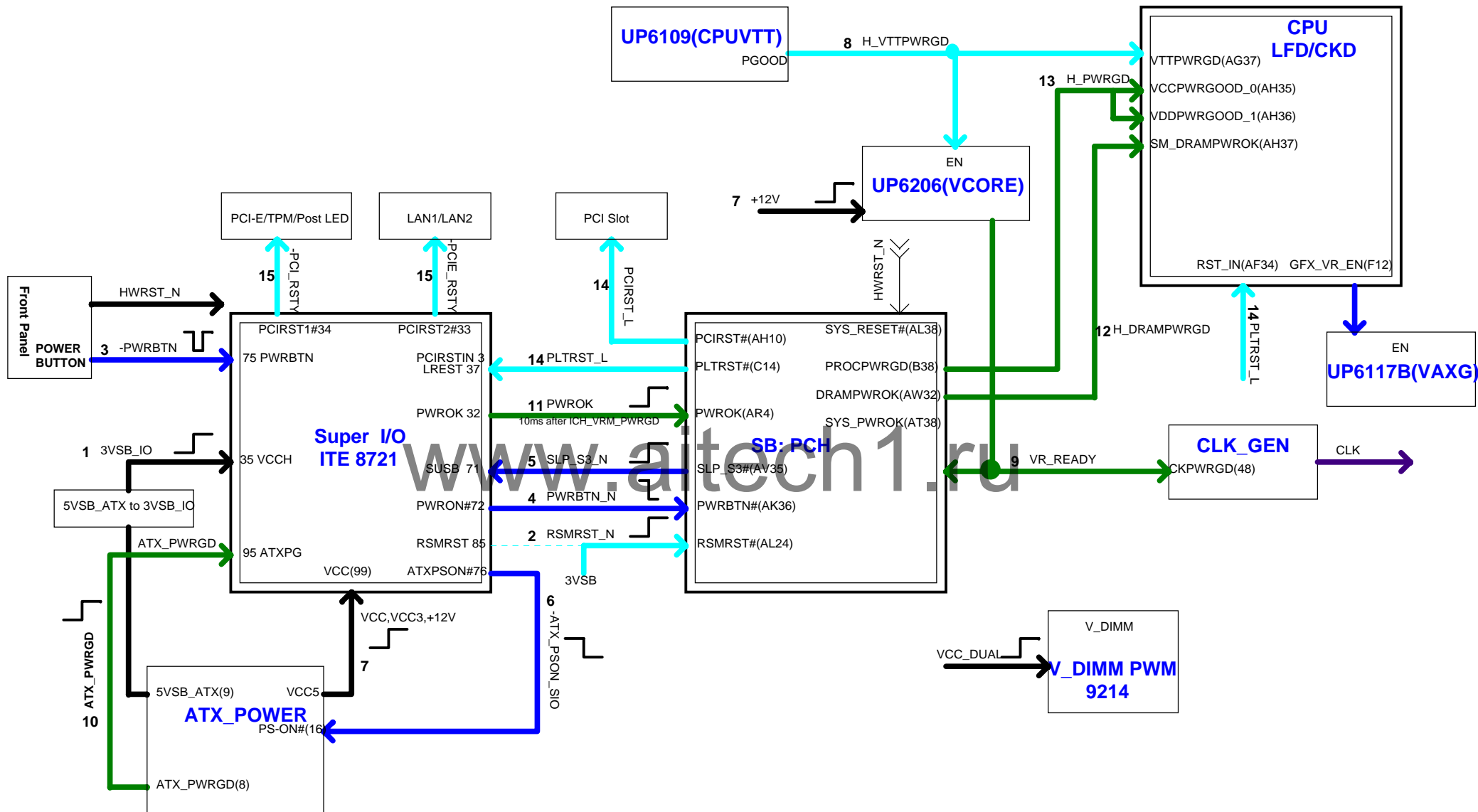
BOM Difference

	RTL8111E-GR 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-04
Cf		
Cg		

Cb







PCH STRAPS TABLE																
	H	L	DESCRIPTION	Default												
PGNT-3	(inter pu)	*Top Boot Block(-0)	A16 SWAP OVERRIDE Low: OVERRIDE	TestPoint												
PGNT-1, PGNT-0	<table border="1"><tr><td>BOOT DEVICE</td><td>GNT0</td><td>GNT1</td></tr><tr><td>LPC</td><td>0</td><td>0</td></tr><tr><td>PCI</td><td>0</td><td>1</td></tr><tr><td>*SPI</td><td>1</td><td>1</td></tr></table>	BOOT DEVICE	GNT0	GNT1	LPC	0	0	PCI	0	1	*SPI	1	1		Inter Pu Hi	SPI
BOOT DEVICE	GNT0	GNT1														
LPC	0	0														
PCI	0	1														
*SPI	1	1														
PGNT-2	(inter pu)	*(-0),Desktop not pull low	DMI AC Coupling Low: Full Voltage Mode	TestPoint												
HDA_SDO	*POWERED BY EPW(-0)	POWERED BY CORE(inter pu)	NAND VCCQ PWR WELL SEL													
HDA_SYNC	*1.5V(-0)	1.8V	OD PLL VR SUPPLY SEL													
SPI_MOSI	*EN(-0)	DIS(inter pu)	TPM FUNCTIONALITY TPM DISABLED WHEN SAMPLED LOW													
NVR_ALE	*(10K)		DANBURY Technology Enable Enable When Sampled High													
NVR_CLE	*(-0)		DMI Termination Voltage DC Coup: TX/RX To VCC Is Sampled High													
INIT3_3V_N		*(-0)	Configurable CPU Output, Stronger If Low													
SPKR	*EN(1K)	DIS	STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).													
PCH_INTVRMEN	*EN(390K)		ENABLE INTERGRATED 1.05V SUS VRM.													
PCH_PU_GP33																
IGC_EN_N		*EN	INTEGRATED CLOCK CHIP ENABLE, Stuff Low For Full Clock Integration Enable.													
VCCVRM_EN GPIO27	*EN(inter pu)	DIS(-0)	OD PLL VR(VccCLK,VccapllEXP, VccFDIPLL,VccSATAPLL; DG P383)													
PCH_GP15	*EN(10K)	DIS	INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) WITH CONFIDENTIALITY													

www

PCI ROUTING

PCI1	AD17	INTA, B, C, D	PREQ-0	PGNT-0
PCI2	AD18	INTB, C, D, A	PREQ-1	PGNT-1

FAN_TAC1	CPU_FAN
FAN_CTL1	CPU_FAN
TMPIN1	SYS_Temp
VIN0	VCORE
VIN1	V_DIMM

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1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

暗BOM叫p (104) Reference

